Analog Vector Generator

VCTR 9850ACDFϕ 8 cycles 5.3 μS

ΔY BLSBS ϕϕϕ ΔY 5 MSBS ΔX 8 LSBS ΔX 5 MSBS

ϕϕ1

ΔX and ΔY are 13 bit two's compliment numbers representing the change from current location. The screen contains ±512 X positions and ±384 Y positions. The hardware allows over-scan to ±768 positions from center. Center screen is ϕϕϕ.

ϕ contains 3 bits of intensity information. If ϕ≤111, the intensity is a four bit number equal to 2ϕ. If ϕ=001, the intensity is the four bit number stored in the Z register by the STAT instruction. If ϕ=00ϕ, the vector is blanked.

HALT 98Fϕ

Z 2 cycles 1.5 μS

Halts execution of the vector generator. Sets halt flag.

SVEϕ 9B5CDFϕ

6 cycles 2.0 μS

= ΔX 5 BBS 01ϕ ΔY 5 BBS

ϕϕ1

ΔX and ΔY are 5 bit two's compliment numbers, representing one-half of the change from current location. See VCTR instruction for further information.
$Z$ is a 4 bit number which is stored in the intensity register. This value is used for the vector intensity whenever the 3 bit $Z$ code in a $VCTR$ or $SVEC$ instruction is $\phi 1$. All 16 codes are permissible.

$EN$, when set to 1, loads the window circuit. This circuit blanks vectors either within the window ($\frac{-1}{5} = 1$) or outside ($\frac{-1}{5} = 0$). $\frac{1}{5}$ determines whether the current location is the upper bound or the lower bound. A complete window is defined by using the instruction twice. Since the limits are stored in an analog manner, the values should be refreshed at least once per frame.

**SCLN** 98E 3 cycles 2 μs

**8 BIT LINEAR SCALE** 111 φ

**BIN SCALE**

BIN scale is a 3 bit number, B, which multiplies all lengths by $2^B$. Linear scale is an 8 bit number, L, which multiplies all lengths by $1 - \frac{1}{2^B}$. I.e. $\phi 0$ is full size, $\phi 1$ is $3/4$ size, $\phi 2$ is half size. For optimum display performance, L should not exceed $\phi 0$.

**CNTR** 98CF 5 cycles 81.9 μs 88 μs

111 100 000 000 000 000

Center beam on screen
JSR 98C DE  5 cycles  3.3 µs

Add 1 0 1
B LSBS  ADD 4 MSBS

Jump to subroutine at address 2*ADD. The address of the next main-line instruction is saved in a four-level stack.

RTS 98DE  4 cycles  2.6 µs

Return from subroutine. The address at the top of the stack is moved to the program counter.

JMP 9BE  3 cycles  2 µs

Add 1 1 1
B LSBS  ADD 4 MSBS

Jump to address 2*ADD and continue executing.

NOTE: All information contained herein is subject to change (and no doubt will) at any time, without warning or notice. The engineer warrants that these instructions are real instructions at this time. This warranty is expressed in lieu of all other warranties, expressed or implied, including the implied warranty of fitness for a particular purpose. This warranty shall not apply to articles which have been altered or abused. This warranty gives you specific legal rights, and you may have other rights which vary from state to state.
VCCTR

The hardware allows overscan to ±1024. It always has—no mods required.

SVEC

A dot \((a_x=0, a_y=0)\) is not allowed. Use either the VCCTR instruction \((a_x=0, a_y=0)\) or use a SVEC of length 2. A vector of length 2 is not noticeable as anything but a dot. The vector macros will generate a VCCTR instruction when \(a_x=0, a_y=0\).

SCAL

Change to read: "Bin scale is a 2 bit number, \(B\) which multiplies all lengths by \(2^B\). This means that a scale factor of 1 is full scale. A scale factor of 0 is double size. A scale factor of 2 is half size, etc."